FIG. 1

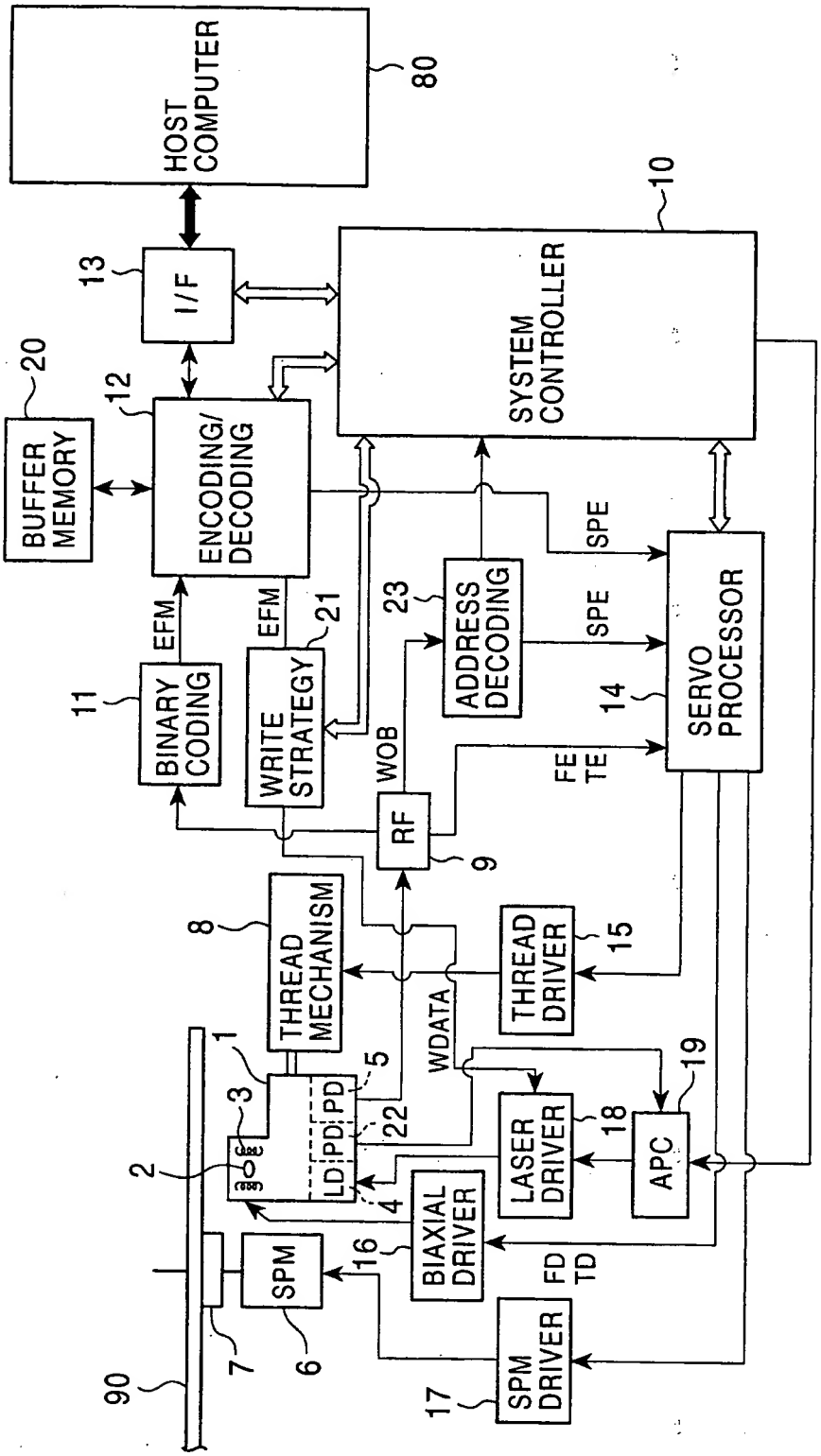
HOST COMPUTER
80
I/F
13
SYSTEM CONTROLLER
10
BUFFER MEMORY
20
ENCODING/ DECODING
12
EFM
EFM
21
23
ADDRESS DECODING
SPE
SPE
SERVO PROCESSOR
14
11
BINARY CODING
WRITE STRATEGY
WOB
FE
TE
RF
9
8
THREAD MECHANISM
THREAD DRIVER
15
WDATA
1
3
5
22
LD
PD
PD
2
4
LASER DRIVER
18
APC
19
BIAXIAL DRIVER
16
FD
TD
SPM
6
7
90
SPM DRIVER
17

FIG. 2

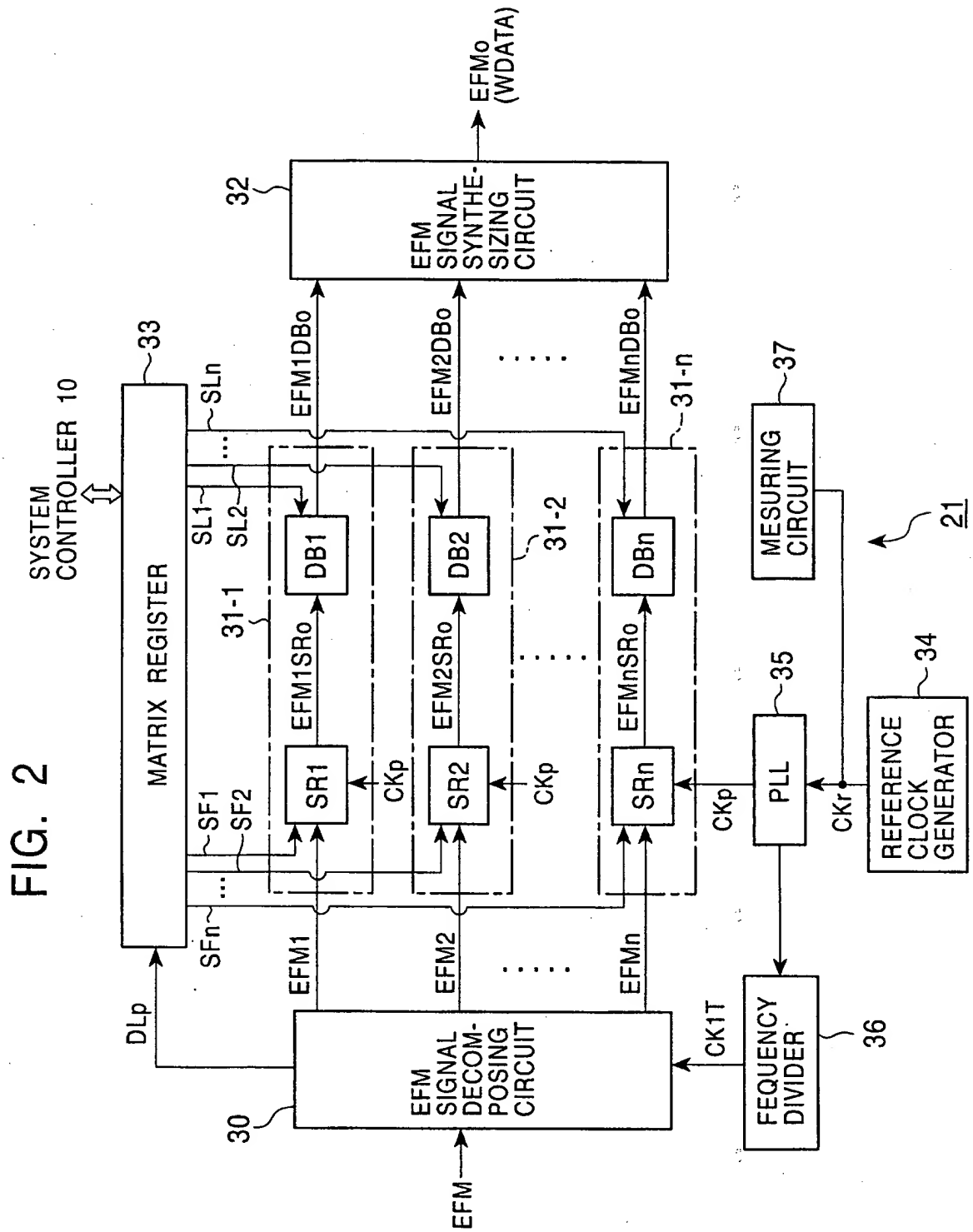
SYSTEM CONTROLLER 10
MATRIX REGISTER
33
SL1
SL2
SLn
SF1
SF2
SFn
31-1
31-2
31-n
DB1
DB2
DBn
SR1
SR2
SRn
EFM1SRo
EFM2SRo
EFMnSRo
EFM1DBo
EFM2DBo
EFMnDBo
CKp
32
EFM SIGNAL SYNTHE-SIZING CIRCUIT
EFMo (WDATA)
EFM1
EFM2
EFMn
DLp
30
EFM SIGNAL DECOM-POSING CIRCUIT
EFM
CK1T
FEQUENCY DIVIDER
36
PLL
35
CKr
REFERENCE CLOCK GENERATOR
34
MESURING CIRCUIT
37
21

FIG. 3

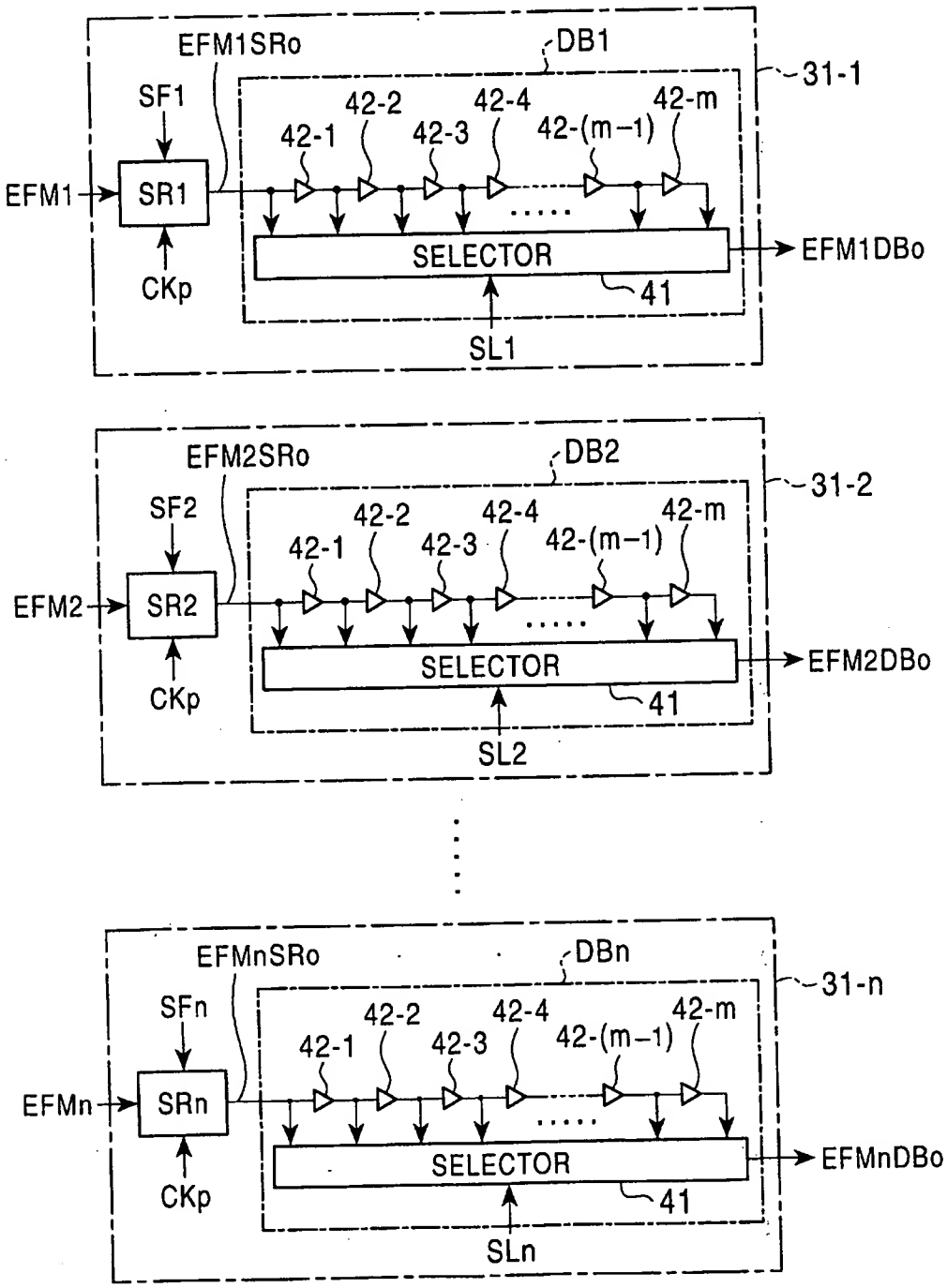
EFM1SRo
DB1
31-1
SF1
42-1
42-2
42-3
42-4
42-(m−1)
42-m
EFM1
SR1
SELECTOR
EFM1DBo
CKp
41
SL1
EFM2SRo
DB2
31-2
SF2
EFM2
SR2
EFM2DBo
SL2
EFMnSRo
DBn
31-n
SFn
EFMn
SRn
EFMnDBo
SLn

FIG. 4

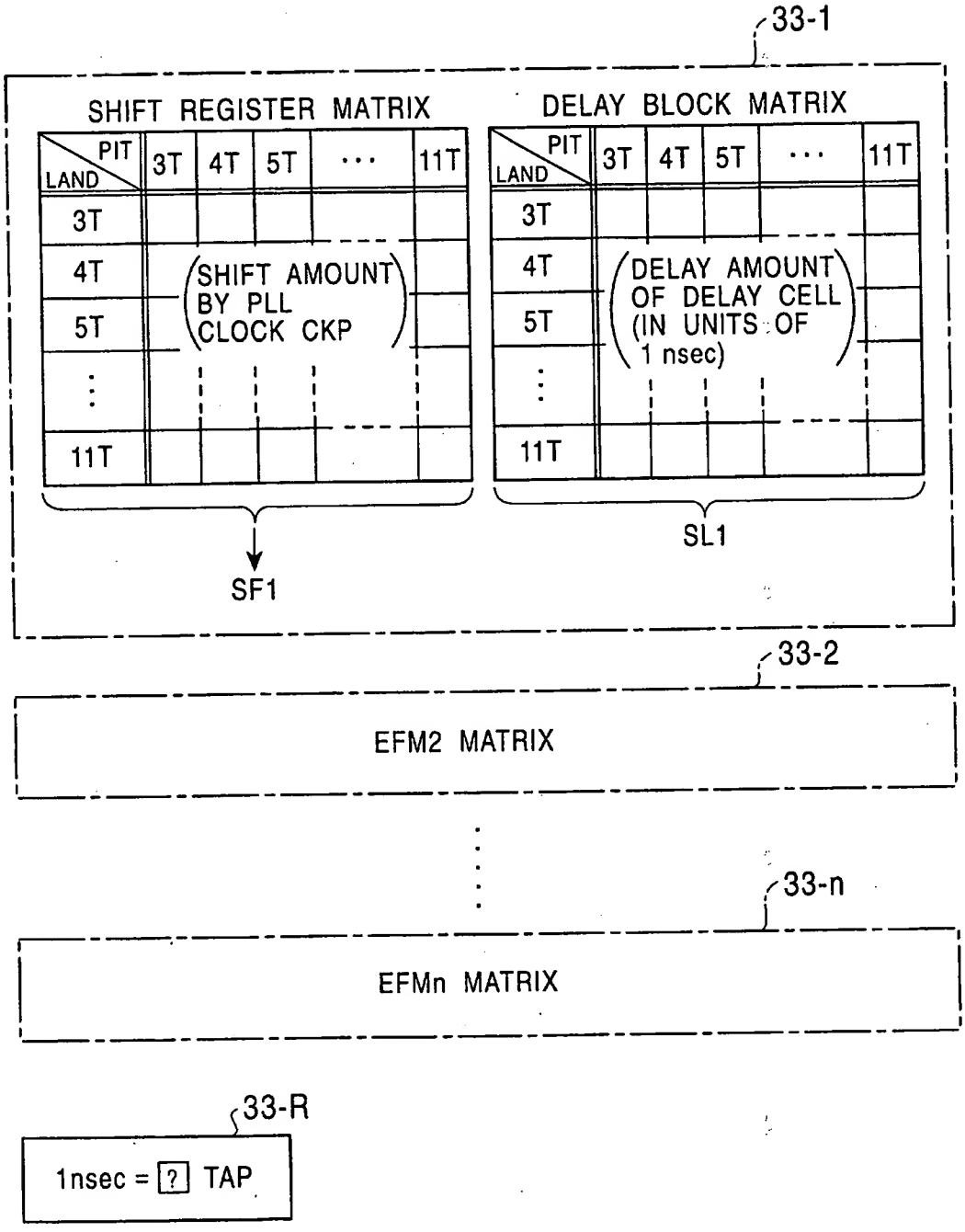
33-1
SHIFT REGISTER MATRIX
PIT
LAND
3T
4T
5T
···
11T
SHIFT AMOUNT BY PLL CLOCK CKP
SF1
DELAY BLOCK MATRIX
DELAY AMOUNT OF DELAY CELL (IN UNITS OF 1 nsec)
SL1
33-2
EFM2 MATRIX
33-n
EFMn MATRIX
33-R
1nsec = ? TAP

FIG. 5

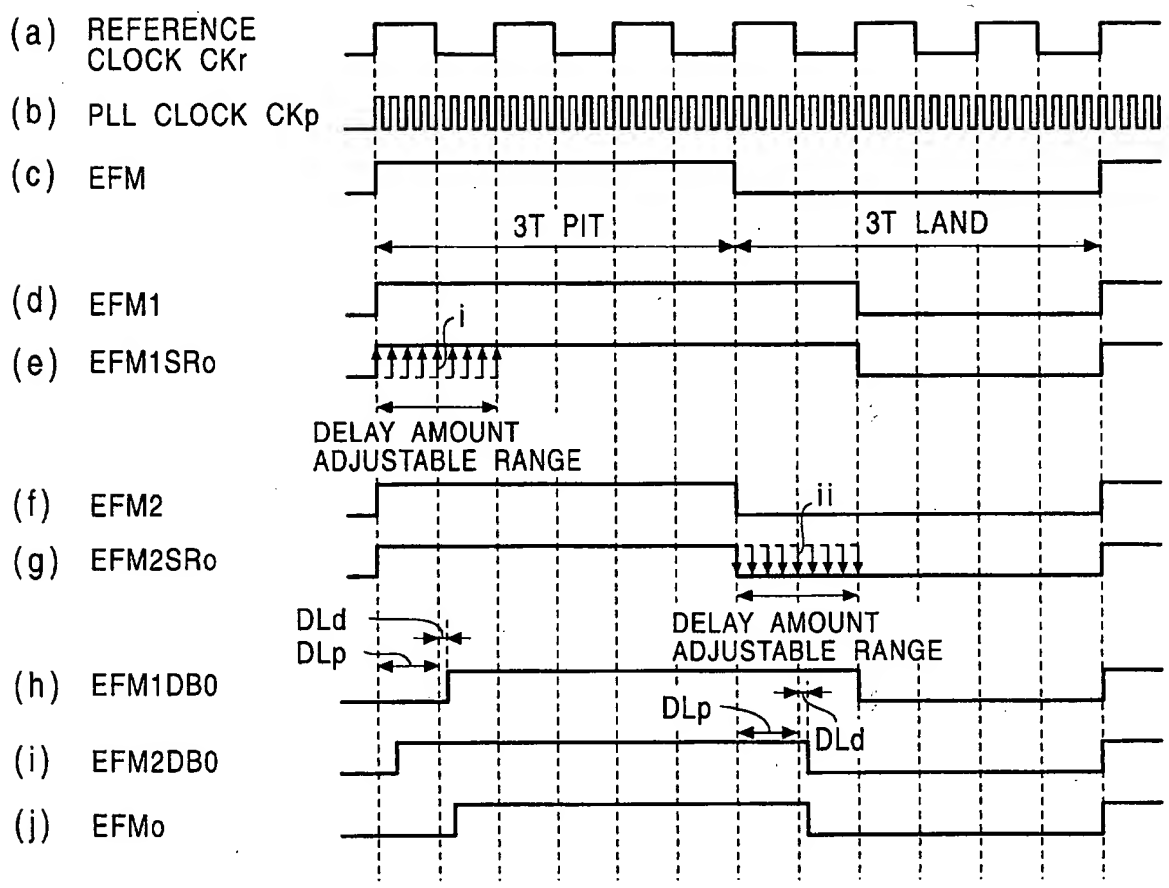
(a) REFERENCE CLOCK CKr
(b) PLL CLOCK CKp
(c) EFM
3T PIT
3T LAND
(d) EFM1
(e) EFM1SRo
i
DELAY AMOUNT ADJUSTABLE RANGE
(f) EFM2
ii
(g) EFM2SRo
DLd
DLp
DELAY AMOUNT ADJUSTABLE RANGE
(h) EFM1DB0
DLp
DLd
(i) EFM2DB0
(j) EFMo

FIG. 6

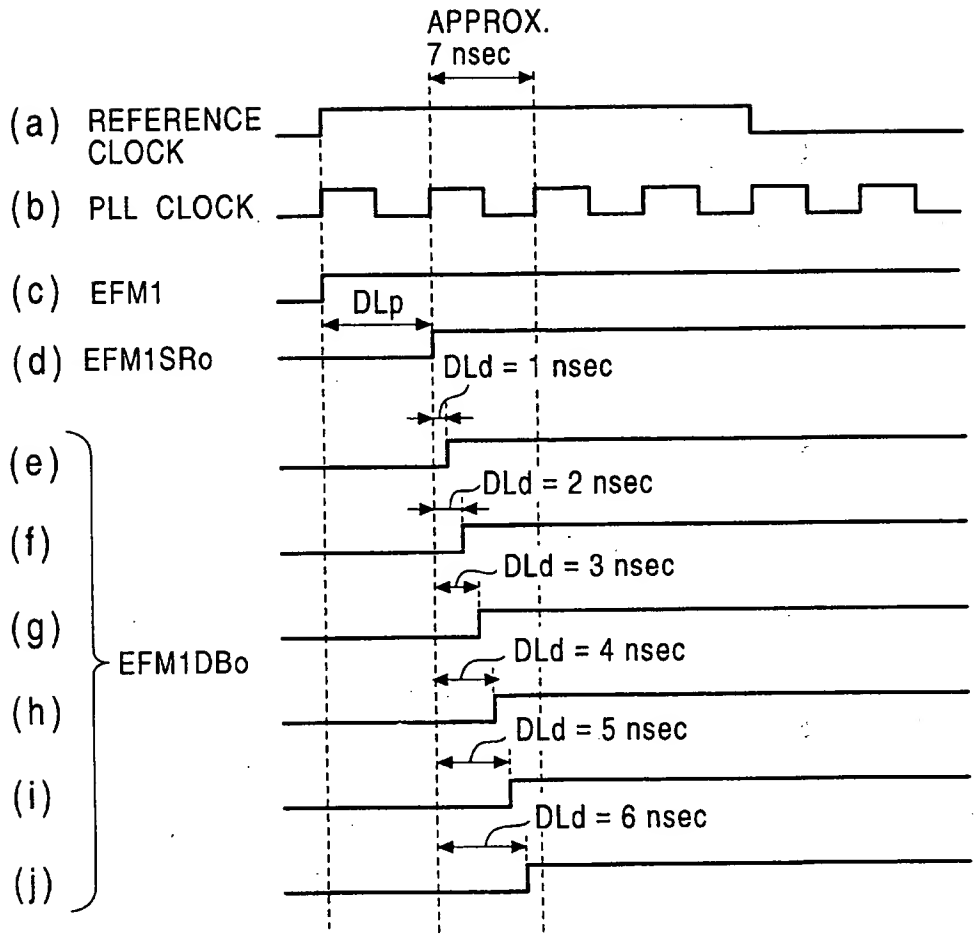
APPROX.
7 nsec
(a) REFERENCE CLOCK
(b) PLL CLOCK
(c) EFM1
DLp
(d) EFM1SRo
DLd = 1 nsec
(e)
DLd = 2 nsec
(f)
DLd = 3 nsec
(g)
DLd = 4 nsec
(h)
DLd = 5 nsec
(i)
DLd = 6 nsec
(j)
EFM1DBo

FIG. 7

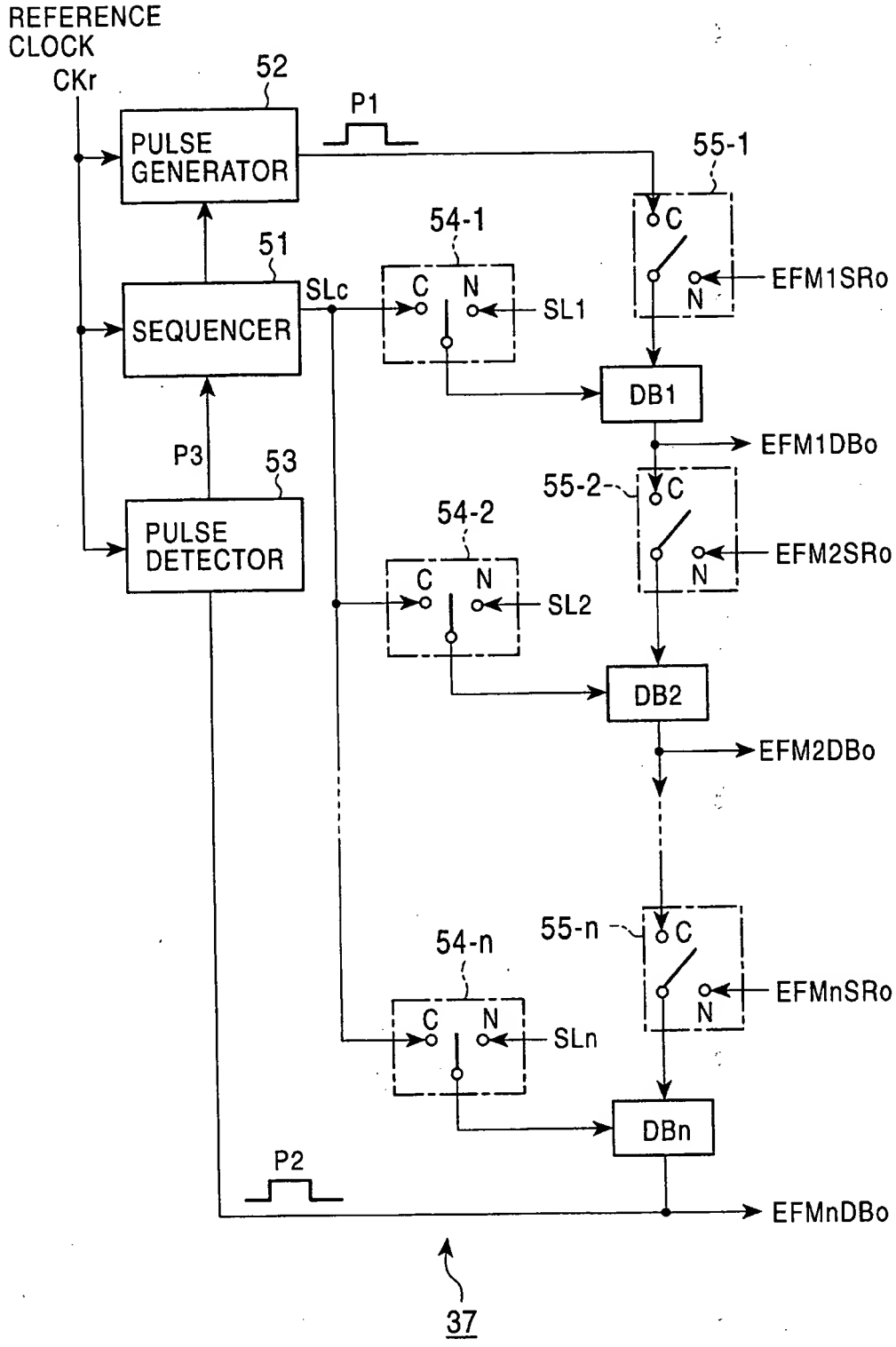
REFERENCE CLOCK
CKr
52
PULSE GENERATOR
P1
55-1
C
N
EFM1SRo
54-1
C
N
SL1
51
SEQUENCER
SLc
DB1
EFM1DBo
P3
53
PULSE DETECTOR
55-2
C
N
EFM2SRo
54-2
C
N
SL2
DB2
EFM2DBo
55-n
C
N
EFMnSRo
54-n
C
N
SLn
DBn
P2
EFMnDBo
37

FIG. 8

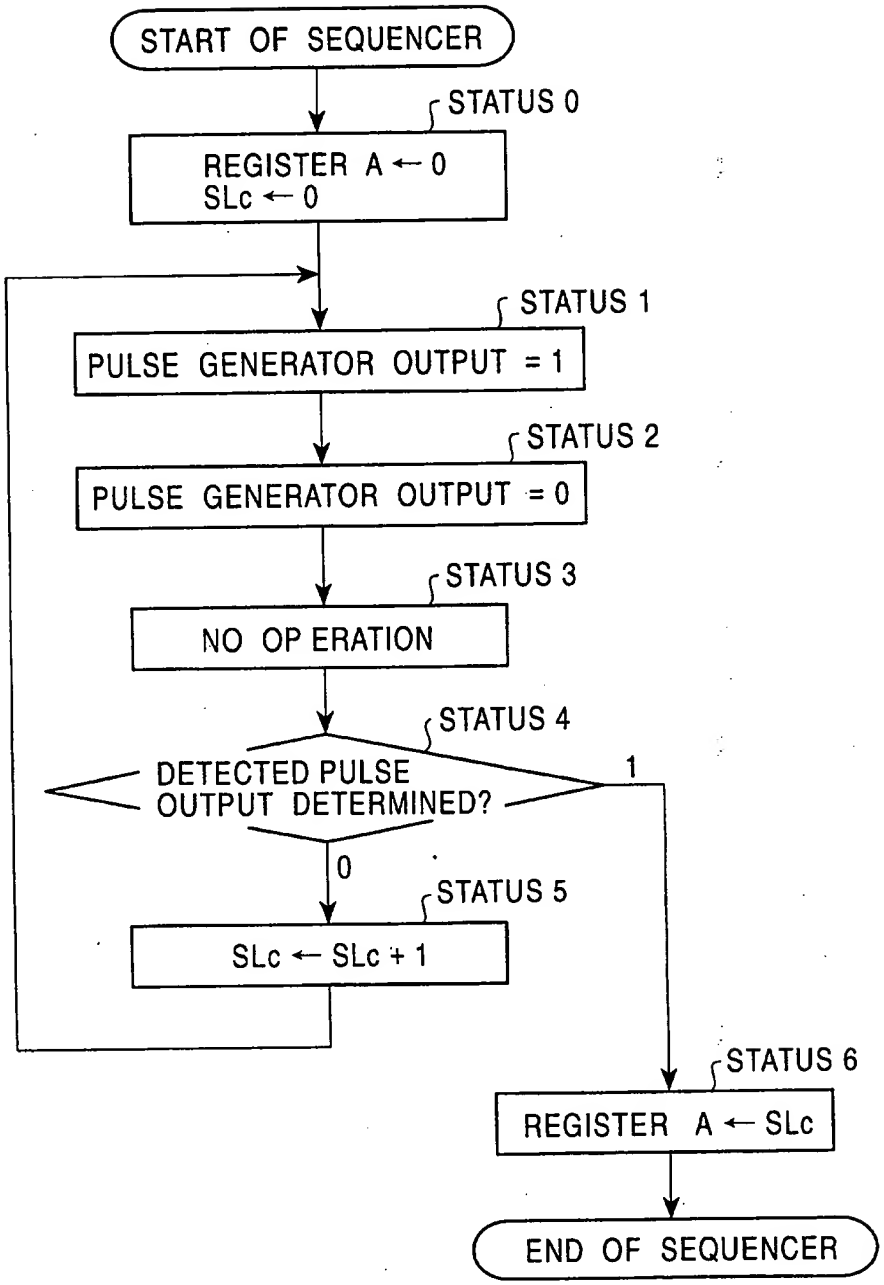
START OF SEQUENCER
STATUS 0
REGISTER A ← 0
SLc ← 0
STATUS 1
PULSE GENERATOR OUTPUT = 1
STATUS 2
PULSE GENERATOR OUTPUT = 0
STATUS 3
NO OP ERATION
STATUS 4
DETECTED PULSE OUTPUT DETERMINED?
1
0
STATUS 5
SLc ← SLc + 1
STATUS 6
REGISTER A ← SLc
END OF SEQUENCER

FIG. 9

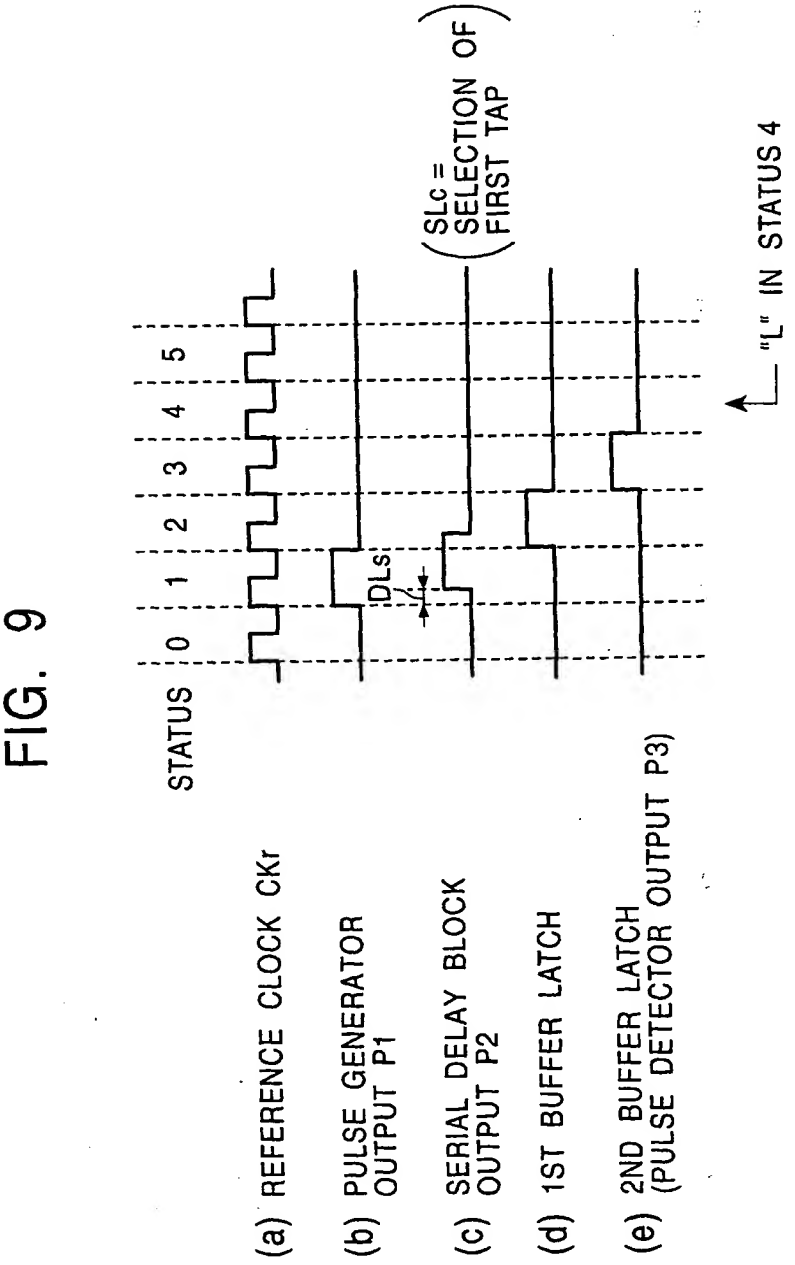
STATUS
0
1
2
3
4
5
(a) REFERENCE CLOCK CKr
(b) PULSE GENERATOR OUTPUT P1
(c) SERIAL DELAY BLOCK OUTPUT P2
(d) 1ST BUFFER LATCH
(e) 2ND BUFFER LATCH (PULSE DETECTOR OUTPUT P3)
DLs
(SLc = SELECTION OF FIRST TAP)
"L" IN STATUS 4

FIG. 10

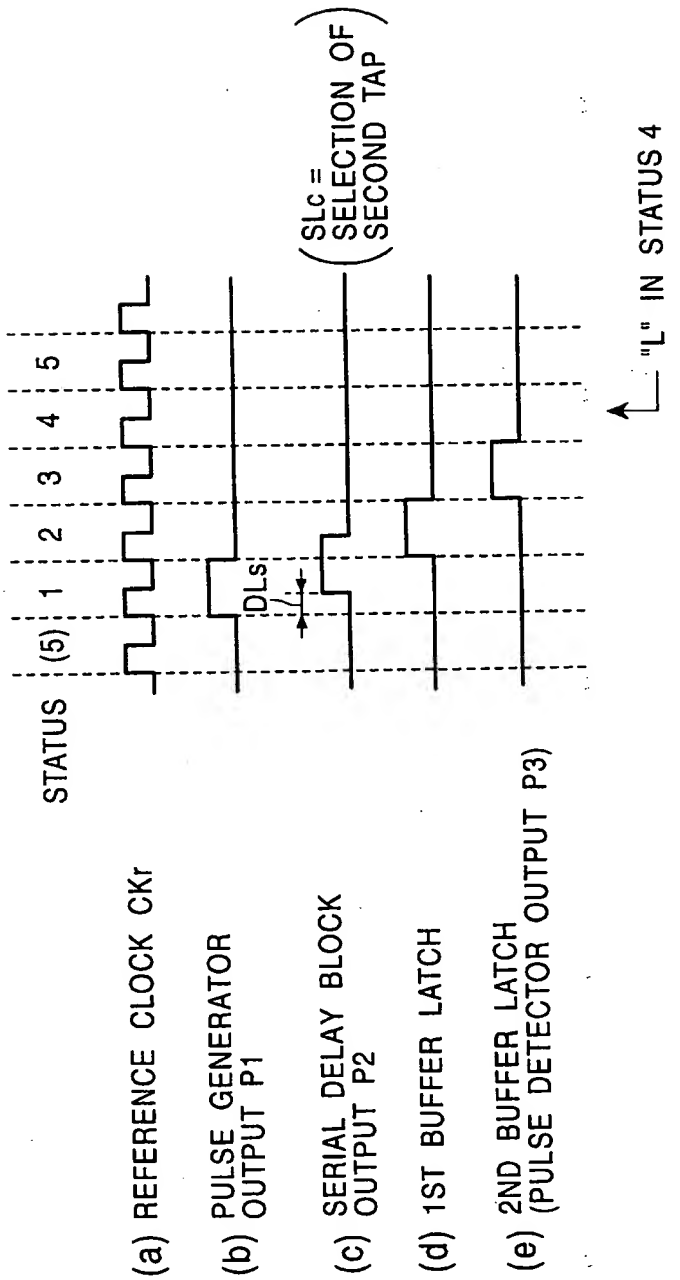
STATUS
(5)
1
2
3
4
5
DLs
SLc = SELECTION OF SECOND TAP
"L" IN STATUS 4
(a) REFERENCE CLOCK CKr
(b) PULSE GENERATOR OUTPUT P1
(c) SERIAL DELAY BLOCK OUTPUT P2
(d) 1ST BUFFER LATCH
(e) 2ND BUFFER LATCH (PULSE DETECTOR OUTPUT P3)

FIG. 11

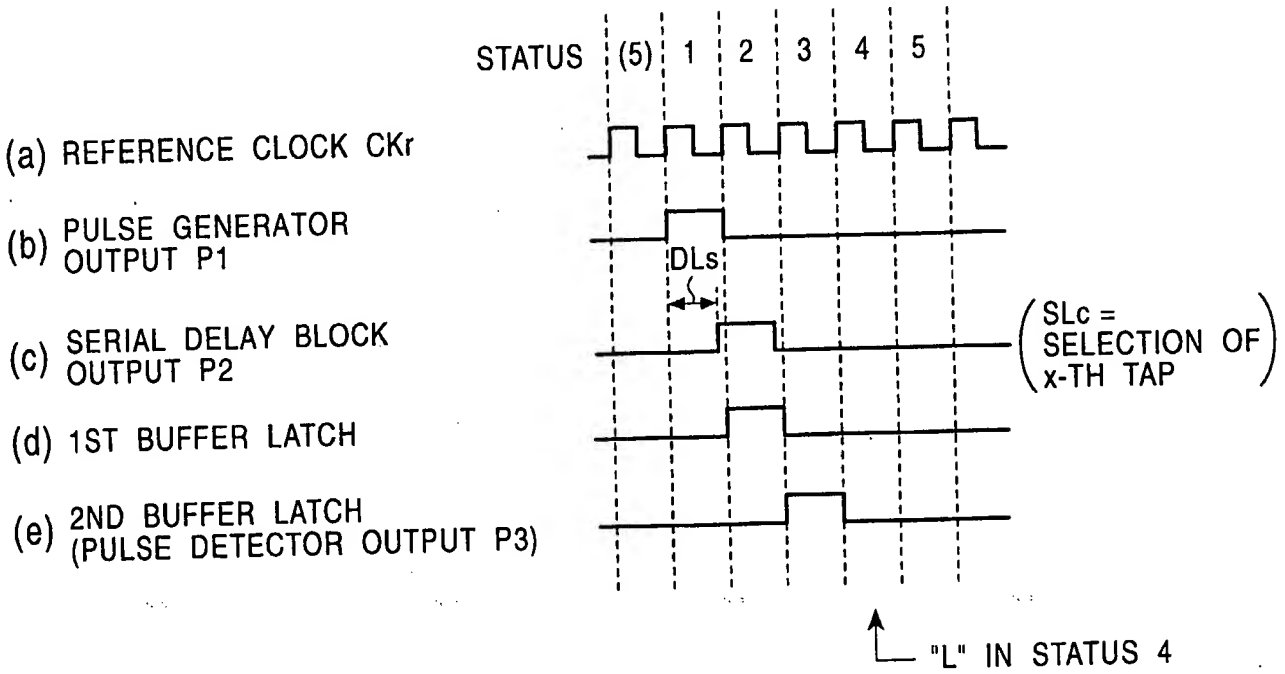
STATUS
(5)
1
2
3
4
5
(a) REFERENCE CLOCK CKr
(b) PULSE GENERATOR OUTPUT P1
DLs
(c) SERIAL DELAY BLOCK OUTPUT P2
SLc = SELECTION OF x-TH TAP
(d) 1ST BUFFER LATCH
(e) 2ND BUFFER LATCH (PULSE DETECTOR OUTPUT P3)
"L" IN STATUS 4

FIG. 12

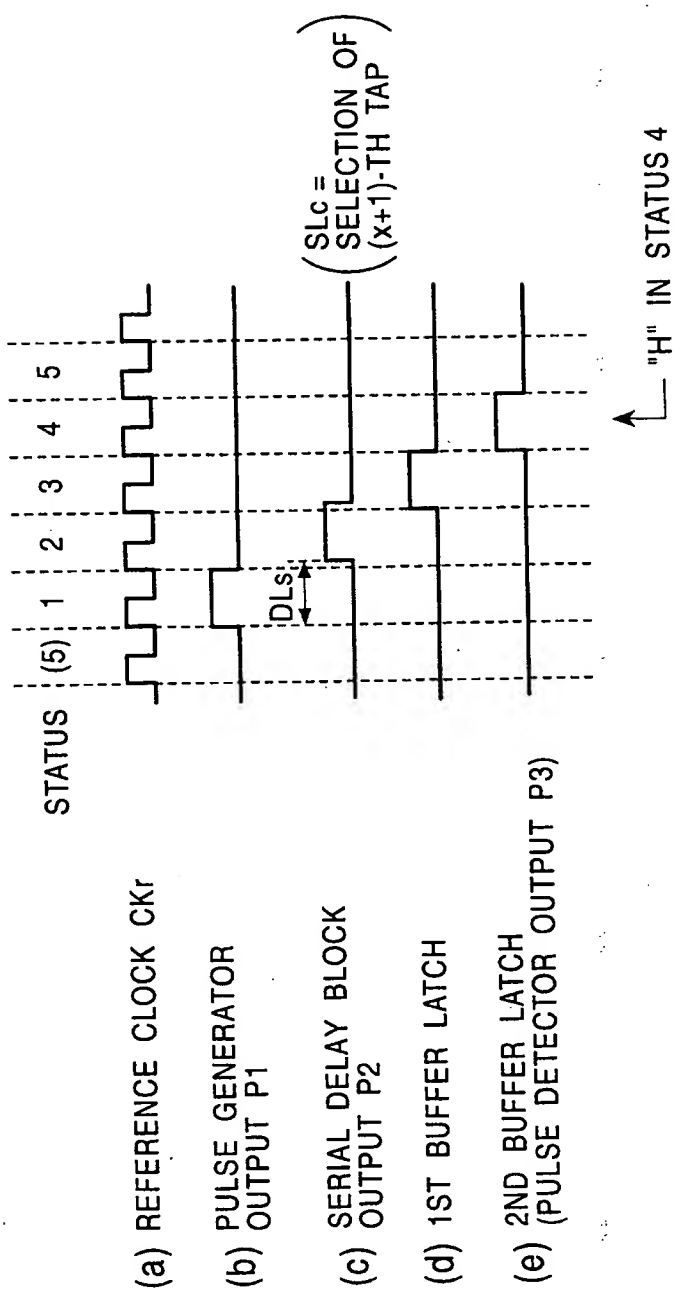
STATUS
(5)
1
2
3
4
5
(a) REFERENCE CLOCK CKr
(b) PULSE GENERATOR OUTPUT P1
DLs
(c) SERIAL DELAY BLOCK OUTPUT P2
(SLc = SELECTION OF (x+1)-TH TAP)
(d) 1ST BUFFER LATCH
(e) 2ND BUFFER LATCH (PULSE DETECTOR OUTPUT P3)
"H" IN STATUS 4

FIG. 13

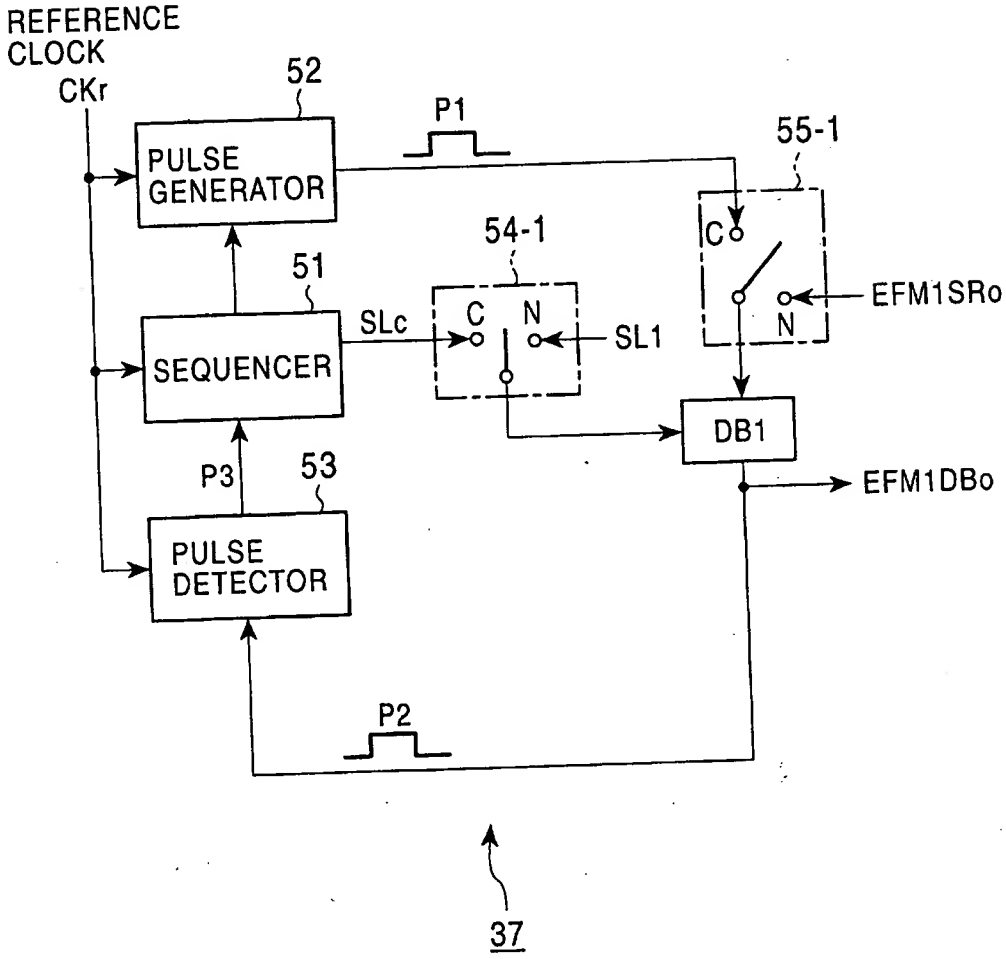
REFERENCE CLOCK
CKr
52
PULSE GENERATOR
P1
55-1
C
N
EFM1SRo
54-1
51
SEQUENCER
SLc
C
N
SL1
DB1
EFM1DBo
P3
53
PULSE DETECTOR
P2
37

FIG. 14

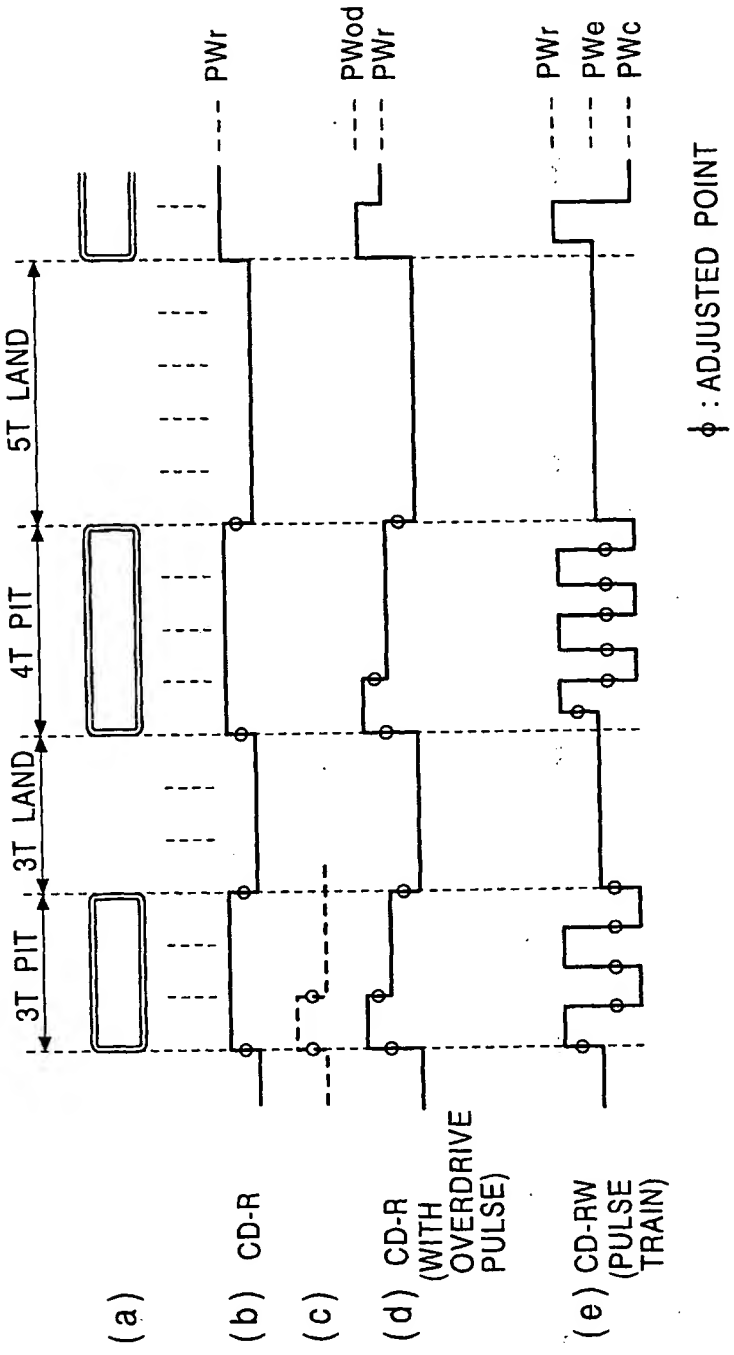
5T LAND
4T PIT
3T LAND
3T PIT
PWr
PWod
PWr
PWr
PWe
PWc
ϕ : ADJUSTED POINT
(a)
(b) CD-R
(c)
(d) CD-R (WITH OVERDRIVE PULSE)
(e) CD-RW (PULSE TRAIN)

FIG. 15

FIG. 16

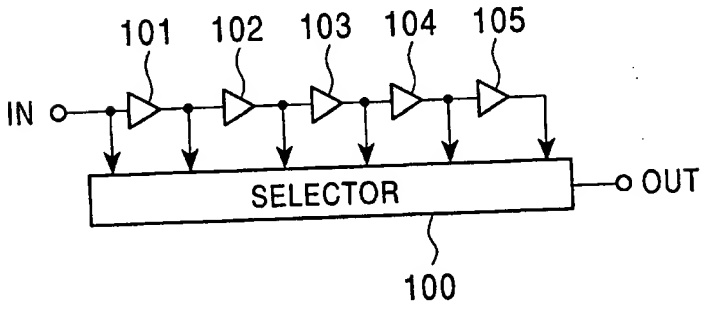
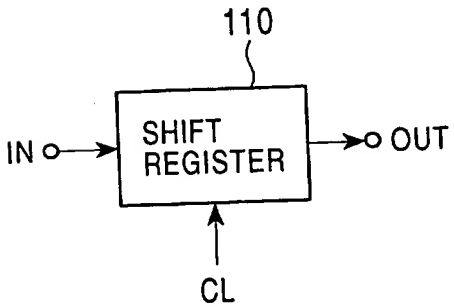
FIG. 17